IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.:	10/091,176	Examiner:	Harrison, Chante
Filed:	March 5, 2002	Group/Art Unit:	2677
Inventor(s):		Atty. Dkt. No:	5181-84600
	Charles Patton		
Title:	PIPELINED 2D VIEWPORT CLIP CIRCUIT		

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313-1450, on the date indicated below.

Mark K. Brightwell

Mar. 20, 2006 (Date) Mark K. Brightwell (Signature)

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal filed January 18, 2006, Appellant presents this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

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I. REAL PARTY IN INTEREST

The subject application is owned by SUN MICROSYSTEMS, INC., a corporation organized and existing under and by virtue of the laws of the State of Delaware, and having its principal place of business at 901 San Antonio Road, Palo Alto, CA 94303, as evidenced by the assignment recorded at Reel 013061, Frame 0090.

II. RELATED APPEALS AND INTERFERENCES

No other appeals, interferences or judicial proceedings are known which would be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 18-40 are pending and rejected. The rejection of claims 18-40 is being appealed. A copy of claims 18-40 is included in the Claims Appendix hereto.

IV. STATUS OF AMENDMENTS

No amendments to the claims have been submitted subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method for comparing a pixel location against a plurality of windows. The method comprises passing the pixel location through a plurality of clip circuits, wherein the clip circuits are connected in a series to form a pipeline, and wherein each clip circuit is a segment of the pipeline (*as disclosed at least at page 5, lines 3-8 (as amended 2/23/2005), and at page 19, lines 1-8, of the specification*).

The method further comprises computing a window result in each clip circuit for the pixel location, wherein each clip circuit is provided data defining a different one of

the plurality of windows, wherein the window result comprises an indication of inclusion of the pixel location within the corresponding one of the plurality of windows (*as disclosed at least at page 19, lines 9-13, of the specification*).

The method further comprises outputting the pixel location and a window word from each clip circuit, wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits except for the last clip circuit in the series, and wherein the window word also comprises any previous window results (*as disclosed at least at page 19, lines 14-19, of the specification*).

The method further comprises examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the windows (*as disclosed at least at page 19, lines 20-22, of the specification*).

Independent claim 26 is directed to a method for comparing a pixel location against a plurality of windows. The method comprises supplying window boundary coordinates for a different one of a plurality of windows to each clip circuit of a plurality of clip circuits connected in a series (*as disclosed at least at page 5, lines 3-8 (as amended 2/23/2005), and at page 19, lines 1-8, of the specification*).

The method further comprises determining inclusion of a pixel in the corresponding window in each clip circuit (*as disclosed at least at page 19, lines 9-13, of the specification*).

The method further comprises passing the pixel and a result of said determining inclusion to a next clip circuit in the series of clip circuits, except for a last clip circuit of the series of clip circuits (*as disclosed at least at page 19, lines 14-19, of the specification*).

Independent claim 34 is directed to a system for determining inclusion of a pixel with respect to each of a plurality of windows. The system comprises a plurality of clip circuits connected in a series (*as disclosed at least at page 5, lines 3-8 (as amended 2/23/2005), and at page 20, lines 20-23, of the specification*).

Each circuit in the series is configured to: (a) receive horizontal and vertical coordinates locating a pixel, (b) receive horizontal and vertical coordinates defining a

different one of a plurality of windows, and (c) compute a window result indicating inclusion of the pixel within the corresponding window defined in (b) (*as disclosed at least at page 21, lines 1-7, of the specification*).

Each circuit in the series except for a last clip circuit in the series is also configured to, (d) pass the horizontal and vertical coordinates of the pixel, the window result computed in (c), and any prior window results to a next clip circuit in the series of clip circuits (*as disclosed at least at page 19, lines 14-19, and at page 21, lines 1-7, of the specification*).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 18-40 are finally rejected in Office Action #4 dated 11/15/2005 under 35 U.S.C. § 103(a) as being unpatentable over Debra Kipping et al. (U.S. Pat. No. 6,831,660), and further in view of C. Narayanaswami, (U.S. Pat. No. 5,883,634).

VII. ARGUMENT

Ground of Rejection:

Claims 18-40 are finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Debra Kipping et al. (U.S. Pat. No. 6,831,660) (hereinafter "Kipping"), and further in view of C. Narayanaswami, (U.S. Pat. No. 5,883,634). Appellant traverses this rejection for the following reasons. Different groups of claims are addressed under their respective subheadings.

Claims 18-25

The Examiner relies on Kipping to teach or render obvious that the clip circuits are connected in a series to form a pipeline, and wherein each clip circuit is a segment of the pipeline, as recited in claim 1. In fact, Kipping and Narayanaswami are both silent on clip circuits connected in a series.

The Examiner at page 2 of Office Action #4 points to Fig. 3, element 310, as teaching clip circuits connected in a series. However, element 310 only shows a box with an internal label "Hardware Clippers 320", and therefore does not indicate any connection between Hardware Clippers 320.

The Examiner at page 8 of Office Action #4 also points to col. 1, lines 45-68, of Kipping as teaching Hardware Clippers 320 connected in a series:

> "With the large amounts of data and computations involved in processing graphics data, especially with three-dimensional applications, many of these computations have been offloaded from the central processing units to a graphics adapter. Within these graphics systems, a graphics pipeline located in the graphics adapter is used to process this graphics data. With a pipeline, the graphics data processing is partitioned into stages of processing elements in which processing data may be executed sequentially by separate processing elements.
>
> Within these processing elements, a clipping function is typically implemented in which pixels for a primitive located within a clip area are rendered, while pixels for the primitive outside of the clip area are not rendered. The hardware implementing the clipping function is often referred to as a hardware clipper. Often, more than one clip area is used to render the correct pixels on a display. With some high-end graphics adapters, multiple hardware clippers are present to clip graphics primitives. Clipping primitives, such as lines and segments, are faster using hardware clippers, rather than software clippers."

It is clear from these two paragraphs that Kipping teaches that processing data may be executed sequentially by separate processing elements, that a clipping function is one of the processing elements, and that the clipping function may use multiple hardware clippers. However, there is no teaching that multiple hardware clippers are connected in a series, nor is there any teaching of each hardware clipper determining a result for a corresponding window of a set of multiple windows. Therefore, Kipping teaches that a plurality of separate processing elements form a pipeline, but Kipping is silent on whether a single processing element such as the clipping function performs the clipping function using multiple clip circuits that are connected in a series to form a pipeline.

Furthermore, Kipping and Narayanaswami either singly or in combination do not teach outputting the pixel location and a window word from each clip circuit, wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits as recited in claim 18. To demonstrate anticipation of these features, the Examiner at page 10 of Office Action #4 points to several paragraphs of Kipping and Narayanaswami as teaching "the clip buffer stores the visibility at each pixel position for each window, and updates the stored data upon any changes by any window as each window makes a comparison to the clip buffer value":

> "Clip buffer 316 contains clip planes, which are used as a mask to clip graphic primitives before the raster stores into the frame buffer 310. Using hardware clip planes is not as fast as the hardware clippers, but it is usually faster than clipping the graphic primitives in software. Raster engine 310 includes hardware clippers 320. A hardware clipper processes graphics data to determine whether the graphics data should be displayed. Before a pixel is written to a frame buffer, such as color frame buffer 312, the location of the pixel is compared to the region extents of the region set for the window clipper. The comparison determines if the location of the pixel is outside, on, or inside the region. In these examples, the pixel is not written to the frame buffer if the address is not contained on or inside the draw region or if the pixel lies on or inside a no draw region." [Kipping: col. 4, lines 52-67]
>
> "Each clipping buffer position contains a value indicating which, if any, window is visible at that point. The clipping buffer value is tested by each particular window and only those matching the clipping buffer value write to the frame buffer." [Narayanaswami: col. 1, lines 34-38]
>
> "The window manager (not show) of the graphics system is notified of any changes to the location, size or existence of all windows on the display. The window clip buffer is initialized to FALSE (obscured) whenever a new window is defined 402. The Window Manager analyzes the regions of the display to determine which are visible whenever a window is moved, created or deleted. The pixels within each of the window's visible regions are next marked as true (visible) creating the final clip mask 404. Any action that changes the positions of

the windows will cause the window clip buffer to be updated." [Narayanaswami: col. 3, lines 38-47]

Clearly, there is no teaching in these portions of Kipping or Narayanaswami cited by the Examiner of a series of clip circuits, nor of passing the pixel location and a window word directly to a next clip circuit in the series, nor that the window word passed between a clip circuit and the next clip circuit also comprises any previous window results. In fact, there is no teaching in Kipping or Narayanaswami of one clip circuit sending any information to another clip circuit.

The Examiner at page 11 of Office Action #4 argues that Kipping and Narayanaswami do teach examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the windows, as cited in claim 1. However, as argued above, Kipping and Narayanaswami do not teach a series of clip circuits, nor a last clip circuit in the series, nor a window word output by the last clip circuit that contains the results from all previous clip circuits in the series. Therefore, Kipping and Narayanaswami do not teach examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the windows, as cited in claim 1.

Claim 25

Claim 25 adds the limitation that the "plurality of clip circuits are identical circuits" to the limitations of claim 18 discussed above. Kipping and Narayanaswami are both silent on identical clip circuits.

Claims 26-33

Kipping and Narayanaswami do not teach a plurality of clip circuits connected in a series, nor passing the pixel and a result of said determining inclusion to a next clip circuit in the series of clip circuits, as claimed in claim 26. Please refer to the arguments above in regards to claim 1, demonstrating that there is no teaching in Kipping and

Narayanaswami of clip circuits connected in a series, nor of a result from any clip circuit of the series being passed to any other clip circuit of the series.

Claims 34-40

Kipping and Narayanaswami do not teach a plurality of clip circuits connected in a series, nor that each circuit in the series is configured to pass the pixel and a result computed and any prior window results to a next clip circuit in the series of clip circuits, as claimed in claim 34. Please refer to the arguments above in regards to claim 1, demonstrating that there is no teaching in Kipping and Narayanaswami of clip circuits connected in a series, nor of a result from any clip circuit of the series being passed to any other clip circuit of the series.

VIII. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 18-40 was erroneous, and reversal of his decision is respectfully requested.

The Commissioner is authorized to charge the appeal brief fee of $330.00 and any other fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-84600/JCH. This Appeal Brief is submitted with a return receipt postcard.

Respectfully submitted,

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IX. CLAIMS APPENDIX

The claims on appeal are as follows.

1. - 17. (Cancelled).

18. (Previously Presented) A method for comparing a pixel location against a plurality of windows, the method comprising:

passing the pixel location through a plurality of clip circuits, wherein the clip circuits are connected in a series to form a pipeline, and wherein each clip circuit is a segment of the pipeline;

computing a window result in each clip circuit for the pixel location, wherein each clip circuit is provided data defining a different one of the plurality of windows, wherein the window result comprises an indication of inclusion of the pixel location within the corresponding one of the plurality of windows;

outputting the pixel location and a window word from each clip circuit, wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits except for the last clip circuit in the series, and wherein the window word also comprises any previous window results; and

examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the windows.

19. (Previously Presented) The method of claim 18, wherein said pixel location comprises a horizontal and a vertical coordinate that define position of said pixel on a screen.

20. (Previously Presented) The method of claim 19, wherein each of the plurality of windows comprises a first horizontal and a second horizontal coordinate and a

first vertical and a second vertical coordinate that define each window's boundaries on the screen.

21. (Previously Presented) The method of claim 20, wherein said computing window result comprises:

computing horizontal inclusion by computing if said horizontal pixel coordinate is located between the first horizontal and the second horizontal coordinate of the corresponding window; and

computing vertical inclusion if said vertical pixel coordinate is located between the first vertical and the second vertical coordinate of the corresponding window.

22. (Previously Presented) The method of claim 21, wherein said computing window result further comprises: setting the indication of inclusion of the pixel to positive if both the horizontal and vertical inclusions are true, and setting the indication of inclusion of the pixel negative if one or more of the horizontal and vertical inclusions are false.

23. (Previously Presented) The method of claim 18, further comprising:

clipping the pixel if said examining determines that the pixel is not included in any of the plurality of windows; and

propagating the pixel if said examining determines that the pixel is included in at least one of the plurality of windows.

24. (Previously Presented) The method of claim 18, wherein said plurality of windows comprise two or more 2-D windows.

25. (Previously Presented) The method of claim 18, wherein said plurality of clip circuits are identical circuits.

26. (Previously Presented) A method comprising:

supplying window boundary coordinates for a different one of a plurality of windows to each clip circuit of a plurality of clip circuits connected in a series;

determining inclusion of a pixel in the corresponding window in each clip circuit; and

passing the pixel and a result of said determining inclusion to a next clip circuit in the series of clip circuits, except for a last clip circuit of the series of clip circuits.

27. (Previously Presented) The method of claim 26, wherein said pixel comprises a horizontal and a vertical coordinate that define position of said pixel on a screen.

28. (Previously Presented) The method of claim 27, wherein each of the plurality of windows comprises a first horizontal and a second horizontal coordinate and a first vertical and a second vertical coordinate that define boundaries of each of the plurality of windows on the screen.

29. (Previously Presented) The method of claim 28, wherein said computing window result comprises:

computing horizontal inclusion by computing if said horizontal pixel coordinate is located between the first horizontal and the second horizontal coordinate of the corresponding window; and

computing vertical inclusion if said vertical pixel coordinate is located between the first vertical and the second vertical coordinate of the corresponding window.

30. (Previously Presented) The method of claim 29, wherein said computing window result further comprises: setting the indication of inclusion of the pixel to positive if both the horizontal and vertical inclusions are true, and setting the indication of inclusion of the pixel negative if one or more of the horizontal and vertical inclusions are false.

31. (Previously Presented) The method of claim 26, further comprising:

clipping the pixel if said examining determines that the pixel is not included in any of the plurality of windows; and

propagating the pixel if said examining determines that the pixel is included in at least one of the plurality of windows.

32. (Previously Presented) The method of claim 26, wherein said plurality of windows comprise two or more 2-D windows.

33. (Previously Presented) The method of claim 26, wherein said plurality of clip circuits are identical circuits.

34. (Previously Presented) A system for determining inclusion of a pixel with respect to each of a plurality of windows, the system comprising:

a plurality of clip circuits connected in a series, wherein each circuit in the series is configured to:

(a) receive horizontal and vertical coordinates locating a pixel,

(b) receive horizontal and vertical coordinates defining a different one of a plurality of windows,

(c) compute a window result indicating inclusion of the pixel within the corresponding window defined in (b), and

except for a last clip circuit in the series,

(d) pass the horizontal and vertical coordinates of the pixel, the window result computed in (c), and any prior window results to a next clip circuit in the series of clip circuits.

35. (Previously Presented) The system of claim 34, wherein a first horizontal and a second horizontal coordinate and a first vertical and a second vertical coordinate corresponding to each window define boundaries of each of the plurality of windows in a two-dimensional space.

36. (Previously Presented) The system of claim 34, wherein the system is further configured to:

clip the pixel if all window results indicate the pixel is not included in any of the plurality of windows; or

propagate the pixel if all window results indicate the pixel is included in at least one of the plurality of windows.

37. (Previously Presented) The system of claim 34, wherein the plurality of windows comprises two or more 2-D windows.

38. (Previously Presented) The system of claim 34, wherein the plurality of clip circuits are identical circuits.

39. (Previously Presented) The system of claim 34, wherein each clip circuit of the plurality of clip circuits is directly connected to the next clip circuit in the series of clip circuits.

40. (Previously Presented) The system of claim 34, wherein the plurality of clip circuits form a pipeline, and each clip circuit is a segment of the pipeline.

X. EVIDENCE APPENDIX

No evidence submitted under 37 CFR §§ 1.130, 1.131 or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

XI. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.